#### DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE – RAIGAD – 402 103 Winter Semester Examination – December – 2018 Course: M. Tech. (Electronics Engineering) Semester: | Subject with Subject Code: Computational Methods (MTEEC101) Marks: 60 Date: 24/12/2018 Time: 3 Hrs. Instructions to the Students 1. Each question carries 12 marks. 2. Attempt any five questions of the following. 3. Illustrate your answers with neat sketches, diagram etc., wherever necessary. 4. If some part or parameter is noticed to be missing, you may appropriately assume it and should mention it clearly. (Marks) a) Use Euler's method and its modified form to obtain y(0.2), y(0.4) and y(0.6) correct to Q.1. three decimal places. Given that $\frac{dy}{dt} = y - x^2$ and y(0)=1. (06)b) What are the types of predictor corrector method? Explain any one in detail. (06) Q.2. a) Discuss the various errors caused in performing numerical calculations. (06) b) Find the value of Sinx= $x - x^3/3! + x^5/5!$ with an absolute error smaller than 0.005 (06)for x=0.2000E<sub>0</sub> and x=0.1276E<sub>2</sub> using normalized floating point arithmetic with 4 digit mantissa. **Q.3.** a) Fit a curve of the type $ae^{-bx}$ for the data given below (06)0.25 0.5 0.75 1.0 1.25 2.02.25 1.5 1:75 2.56.8 0.42 0.09 0.03 1.7 1.0 0.26 0.140.04 b) Explain Scatter diagram and fitting of straight line with the help of least squares method. (06)a) Give the Comparison of various Iterative methods. (06) Q.4. (06) b) Find the root of equation $x \sin x + \cos x = 0$ by false position method. (06)**Q.5.** a) What are finite differences? Explain forward, backward and central difference.

Solve the differential equation y' = x+y with y(0)=1,  $x \in [0,1]$  by Taylor's series (06) (06)

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Q.6. a) Given the following table of values

X	0.4	0.5	0.7	0.8
F(x)	-0.916	-0.693	-0.357	-0.223

(06)

Calculate the value of f(0.6) using Lagrange's interpolation

b) Evaluate the following equation using Trapezoidal rule, giving the answers to three decimal places (06)

 $\int_0^1 \frac{2}{1+x^2} \mathrm{d} x$ 



## DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE – RAIGAD – 402 103 Winter Semester Examination – December – 2018

Branch: M.Tech. (Electronics Engineering)Semester: ISubject with Subject Code:- Microelectronics (MTEEC102)Time: 3 Hrs.Marks: 60Date: 27/12/2018

#### Instructions to the Students

1. Each question carries 12 marks.

2. Attempt any five questions of the following.

3. Illustrate your answers with neat sketches, diagram etc., wherever necessary.
4. If some part or parameter is noticed to be missing, you may appropriately assume it and should the should the should be missing.

mention it clearly.

## (Marks)

0.1.	a) Draw and explain the MOS diffusion capacitance model.	(06)
	b) Explain the operation of a tri state inverter.	(06)
0.2.	a) Explain photolithography process in CMOS fabrication.	(06)
¥	b) Explain Gate and Source/Drain in formation in CMOS.	(06)
0.3.	a) What is layout design? What are its approaches? Explain.	(06)
Q.51	b) Discuss CMOS process enhancements.	(06)
0.4.	a) What is design margin? Explain.	(06)
¥	b) Explain RC delay model.	(06)
0.5	a) Explain CMOS multiplexers	(06)
Q.3.	b) Discuss static CMOS family.	(06)
0.6	a) Explain BiCMOS circuits.	(06)
~	b) Explain CMOS inverter as an amplifier.	(06)

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## DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, » LONERE - RAIGAD - 402 103 Winter Semester Examination – December 2018

Branch: M. Tech. (Specialization)	Semester: Log
Subject with Subject Code: - VLSI	System Design (MTEEC103)
Date:- 29-12-2018	Marks: 60 Tu

Instructions to the Students

1. Each question carries 12 marks.

2. Attempt any five questions of the following.

3. Illustrate your answers with neat sketches, diagram etc., wherever necessary.

4. If some part or parameter is noticed to be missing, you may appropriately assume it and should mention it clearly.

Time: 3 Hrs

- Write scalable design rules and layout design rules. (06) Q.No.1 a)
  - Draw layout for NAND gate using CMOS transistors. (06)b)
- Define noise margin. Explain low noise and high noise margin (06)Q.No.2 a) with transistor characteristics of CMOS inverter.
  - What is structure of different cascade voltage switch logic (06)b) (DCVSL)? Explain it and draw a schematic for two input AND/NAND gate in DCVSL.
- Explain different types of Latches: dynamic latch, multiplexed (12) **Q.No.3** dynamic latch and quasi-static latch.

Q.No.4

a)





- Compare design of 4:1 multiplexer using CMOS logic and switch (06) b) logic.
- **O.No.5**
- What is the condition to get equal rise and fall times in general (06) a) (e.g. Inverter, NAND gate).
  - Write different floorplanning methods and design process. (06)(b)
- Explain with neat diagram Register Transfer Design. (06)O.No.6 a) (06)
  - Explain in detail memory cell and arrays b)

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# DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE – RAIGAD – 402 103 Winter Semester Examination –Dec 2018 N.

Branch: M.Tech. (Electronics)		Semester: I	
Subject: Medical Electronics Date:- 1/1/2019	Marks: 60	Subject Code WITEBEI14D	
nstructions to the Students 1. Figures to the right indicate the 2. Attempt any five questions of t 3. Illustrate your answers with new 4. If some part or parameter is n mention it clearly.	full marks. he following. at sketches, diagram, o oticed to be missing,	etc., wherever necessary. you may appropriately assume it and should	
).1 Attempt any two	5025	(12)	
<ul> <li>b) With neat sketch, explain</li> <li>c) How the therapeutic equining in detail?</li> <li>Attempt any two</li> </ul>	diagram of the X pment are classifie	-ray image intensifier?. d? Explain any therapeutic equipment (12)	
<ul> <li>a) List the different surface electron</li> <li>b) Explain the different electron</li> <li>c) What are the voltage range ,</li> </ul>	ctrodes and explain des used for ECG i frequency range us	n them in details . neasurement? sed for ECG, EMG, and EEG signals.	
<ul> <li>2.3 Answer the following</li> <li>a) What are different selection</li> <li>biomedical applications?</li> <li>b) Draw and explain the different</li> </ul>	on factors for trans ferent temperature	(12) ducers used for transducers in details?	
Q.4 Answer the following a) Draw and explain block c	liagram of man ins	(12) trument system?	
b) Draw and explain block of the EEG signals?	hagram of EEO III	actime used for recording and proving	
Q.5 Answer the following	in a datail	(12)	
b) Explain the operating pri neat diagram. Specify the tr	nciple of ultrasoni ansducer and oper	c blood flow measurement along with ating frequency of measuring signal.	
Q.6. Answer the following		(12)	
a) Comment on Macroshoc b) What are the different el equipments?	k and Microshock lectrical accident p	hazards revention methods used in medical	
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DR.	BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE	- RAIGAD
	HINTER DEMOSTER EXAMINATION DECEMBER 2010	
Branc Subje	h: M.Tech. (Electronics Engineering) Sem ct with Subject Code: Elective II (Embedded System Design), MT	ester: 1 EEE125A
Date:	03/01/2019 Marks: 60 Time: 03	Hrs.
Instruc	tions to the Students	1.501530
	<ol> <li>Each question carries 12 marks.</li> <li>Attempt any five questions of the following.</li> <li>Illustrate your answers with neat sketches, diagram etc., wherever necessary.</li> <li>If some part or parameter is noticed to be missing, you may appropriately assume it a mention it clearly.</li> </ol>	nd should
		Marks)
		188
Q.1. a repres archite	a) What is the difference between big – endian and little - endian data entation? Explain the difference between Harvard and Von- Neuman ecture.	(06)
	MANER EST EST STATISTICS STATES	1
b) Wri 3X+8Y	te ARM based assembly language program to implement the equation	(06)
Q.2.	a) What is Bus Protocols? Explain a typical microprocessor bus.	(06)
b) Wh	at is switch bouncing? How you can eliminate this?	(06)
Q.3.	a) what is compilation process? How you will compile Arithmetic Expr	ession? (06)
b) Hov the fa	v you can control power consumption in embedded system? What are ctors that contribute to the energy consumption of the program.	(06)
Q.4.	a) what is scheduling? How priority driven scheduling is carried out?	(06)
b) Exp the op	lain the interprocessor communication mechanism provided by erating system.	(06)
Q.5. a Contro	a) what is performance analysis? Explain single threaded versus multi- ol of an accelerator.	threaded (06)
imple	b) What are the different types of interconnection networks for mentation of distributed embedded systems, explain it.	(06)
Q.6.	a) Explain successive refinement design methodology for embedded sy	stems. (06)
b	) What is systems – on – silicon? Explain with the help of example.	(06)

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